description

The TL783 is an adjustable three-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary-breakdown and thermal-runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if ADJ is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

The TL783C is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

Available Options

<table>
<thead>
<tr>
<th>T_J</th>
<th>Packaged Device</th>
<th>Heat-Sink Mounted (KC)</th>
<th>Chip Form (Y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0°C to 125°C</td>
<td>TL783CKC</td>
<td>TL783CCKC</td>
<td>TL783Y</td>
</tr>
</tbody>
</table>

Chip forms are tested at 25°C.
**functional block diagram**

```
V_I

Error Amplifier

IN

Protection Circuit

OUT

V_O = V_{ref} \left( 1 + \frac{R_2}{R_1} \right)

V_{ref}

R_1

R_2

ADJ

V_O
```

**absolute maximum ratings over operating temperature range (unless otherwise noted)**†

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input-to-output differential voltage, V_I – V_O</td>
<td></td>
<td>125</td>
<td>V</td>
</tr>
<tr>
<td>Operating free-air, T_A; case, T_C; or virtual junction, T_J, temperature</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Package thermal impedance, θ_{JA} (see Notes 1 and 2)</td>
<td></td>
<td>22</td>
<td>°C/W</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds</td>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, T_{stg}</td>
<td></td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**NOTES:**

1. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

2. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input-to-output voltage differential, V_I – V_O</td>
<td></td>
<td>125</td>
<td>V</td>
</tr>
<tr>
<td>Output current, I_O</td>
<td>15</td>
<td>700</td>
<td>mA</td>
</tr>
<tr>
<td>Operating virtual junction temperature, T_J</td>
<td>TL783C</td>
<td>0</td>
<td>125°C</td>
</tr>
</tbody>
</table>
electrical characteristics at $V_I - V_O = 25\,V$, $I_O = 0.5\,A$, $T_J = 0^\circ\text{C}$ to $125^\circ\text{C}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS†</th>
<th>TL783C</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage regulation‡</td>
<td>$V_I - V_O = 20,V$ to $125,V$, $P \leq$ rated dissipation</td>
<td>$T_J = 25^\circ\text{C}$</td>
<td>MIN 0.001</td>
</tr>
<tr>
<td></td>
<td>$T_J = 0^\circ\text{C}$ to $125^\circ\text{C}$</td>
<td></td>
<td>TYP 0.004</td>
</tr>
<tr>
<td>Ripple rejection</td>
<td>$\Delta V_I(PP) = 10,V$, $V_O = 10,V$, $f = 120,\text{Hz}$</td>
<td></td>
<td>MIN 66</td>
</tr>
<tr>
<td>Output voltage regulation</td>
<td>$I_O = 15,\text{mA}$ to $700,\text{mA}$, $T_J = 25^\circ\text{C}$</td>
<td>$V_O \leq 5,V$</td>
<td>MIN 7.5</td>
</tr>
<tr>
<td></td>
<td>$V_O \geq 5,V$</td>
<td></td>
<td>TYP 0.15%</td>
</tr>
<tr>
<td></td>
<td>$I_O = 15,\text{mA}$ to $700,\text{mA}$, $P \leq$ rated dissipation</td>
<td>$V_O \leq 5,V$</td>
<td>MIN 20</td>
</tr>
<tr>
<td></td>
<td>$V_O \geq 5,V$</td>
<td></td>
<td>TYP 0.3%</td>
</tr>
<tr>
<td>Output voltage change with temperature</td>
<td></td>
<td></td>
<td>MIN 0.4%</td>
</tr>
<tr>
<td>Output voltage long-term drift</td>
<td>$1000,\text{hours}$ at $T_J = 125^\circ\text{C}$, $V_I - V_O = 125,V$</td>
<td></td>
<td>MIN 0.2%</td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>$f = 10,\text{Hz}$ to $10,\text{kHz}$, $T_J = 25^\circ\text{C}$</td>
<td></td>
<td>MIN 0.03%</td>
</tr>
<tr>
<td>Minimum output current to maintain regulation</td>
<td>$V_I - V_O = 125,V$</td>
<td></td>
<td>MIN 15</td>
</tr>
<tr>
<td>Peak output current</td>
<td>$V_I - V_O = 25,V$, $t = 1,\text{ms}$</td>
<td></td>
<td>MIN 1100</td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 15,V$, $t = 30,\text{ms}$</td>
<td></td>
<td>MIN 715</td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 25,V$, $t = 30,\text{ms}$</td>
<td></td>
<td>MIN 700</td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 125,V$, $t = 30,\text{ms}$</td>
<td></td>
<td>MIN 700</td>
</tr>
<tr>
<td>ADJ input current</td>
<td></td>
<td></td>
<td>MIN 83</td>
</tr>
<tr>
<td>Change in ADJ input current</td>
<td>$V_I - V_O = 15,V$ to $125,V$, $I_O = 15,\text{mA}$ to $700,\text{mA}$, $P \leq$ rated dissipation</td>
<td></td>
<td>MIN 0.5</td>
</tr>
<tr>
<td>Reference voltage (OUT to ADJ)</td>
<td>$V_I - V_O = 10,V$ to $125,V$, $I_O = 15,\text{mA}$ to $700,\text{mA}$, $P \leq$ rated dissipation, See Note 3</td>
<td></td>
<td>MIN 1.2</td>
</tr>
</tbody>
</table>

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTE 3: Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.
### TL783 HIGH-VOLTAGE ADJUSTABLE REGULATOR


#### electrical characteristics at $V_I - V_O = 25 \text{ V}, I_O = 0.5 \text{ A}, T_J = 25^\circ\text{C}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS†</th>
<th>TL783Y</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage regulation‡</td>
<td>$V_I - V_O = 20 \text{ V to 125 V}, P \leq \text{rated dissipation}$</td>
<td>0.001</td>
<td>%/V</td>
</tr>
<tr>
<td>Ripple rejection</td>
<td>$\Delta V_I(PP) = 10 \text{ V}, V_O = 10 \text{ V}, f = 120 \text{ Hz}$</td>
<td>76</td>
<td>dB</td>
</tr>
<tr>
<td>Output voltage regulation</td>
<td>$I_O = 15 \text{ mA to 700 mA}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_O \leq 5 \text{ V}$</td>
<td>7.5</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_O \geq 5 \text{ V}$</td>
<td>0.15%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_O = 15 \text{ mA to 700 mA}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_O \leq 5 \text{ V}$</td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_O \geq 5 \text{ V}$</td>
<td>0.3%</td>
<td></td>
</tr>
<tr>
<td>Output voltage change</td>
<td></td>
<td>0.4%</td>
<td></td>
</tr>
<tr>
<td>with temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>$f = 10 \text{ Hz to 10 kHz}$</td>
<td>0.003%</td>
<td></td>
</tr>
<tr>
<td>Peak output current</td>
<td>$V_I - V_O = 25 \text{ V}$</td>
<td>1100</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$t = 1 \text{ ms}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 15 \text{ V}$</td>
<td>715</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t = 30 \text{ ms}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 25 \text{ V}$</td>
<td>900</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t = 30 \text{ ms}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_I - V_O = 125 \text{ V}$</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>ADJ input current</td>
<td></td>
<td>83</td>
<td>µA</td>
</tr>
<tr>
<td>Change in ADJ input current</td>
<td>$V_I - V_O = 15 \text{ V to 125 V}$</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$I_O = 15 \text{ mA to 700 mA}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$P \leq \text{rated dissipation}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference voltage (OUT to ADJ)</td>
<td>$V_I - V_O = 10 \text{ V to 125 V}$</td>
<td>1.27</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_O = 15 \text{ mA to 700 mA}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$P \leq \text{rated dissipation}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Note 3</td>
<td></td>
<td></td>
</tr>
</tbody>
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NOTE 3: Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.
TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT

vs

INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

Figure 1

OUTPUT CURRENT LIMIT

vs

INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

Figure 2

OUTPUT CURRENT LIMIT

vs

TIME

Figure 3

RIPPLE REJECTION

vs

OUTPUT VOLTAGE

Figure 4
TYPICAL CHARACTERISTICS†

**RIPPLE REJECTION vs OUTPUT CURRENT**

![Figure 5](image1)

- $V_{I(AV)} = 25\, \text{V}$
- $\Delta V_{I(PP)} = 10\, \text{V}$
- $V_O = 10\, \text{V}$
- $f = 120\, \text{Hz}$
- $C_O = 0$
- $T_J = 25^\circ\text{C}$

**Figure 5**

**RIPPLE REJECTION vs FREQUENCY**

![Figure 6](image2)

- $V_{I(AV)} = 25\, \text{V}$
- $\Delta V_{I(PP)} = 10\, \text{V}$
- $V_O = 10\, \text{V}$
- $I_O = 500\, \text{mA}$
- $T_J = 25^\circ\text{C}$
- $C_O = 10\, \mu\text{F}$

**Figure 6**

**OUTPUT IMPEDANCE vs FREQUENCY**

![Figure 7](image3)

- $V_I = 35\, \text{V}$
- $V_O = 10\, \text{V}$
- $I_O = 500\, \text{mA}$
- $T_J = 25^\circ\text{C}$

**Figure 7**

**REFERENCE VOLTAGE vs VIRTUAL JUNCTION TEMPERATURE**

![Figure 8](image4)

- $V_I = 20\, \text{V}$
- $I_O = 15\, \text{mA}$

**Figure 8**

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.
TYPICAL CHARACTERISTICS

INPUT CURRENT AT ADJ VS VIRTUAL JUNCTION TEMPERATURE

FDJ = 25 V
VO = Vref
IO = 500 mA

Figure 9

DROP OUT VOLTAGE VS VIRTUAL JUNCTION TEMPERATURE

\[ \Delta V_O = 100 \text{ mV} \]

IO = 700 mA
IO = 600 mA
IO = 500 mA
IO = 250 mA
IO = 100 mA
IO = 15 mA

Figure 10

OUTPUT VOLTAGE DEVIATION VS VIRTUAL JUNCTION TEMPERATURE

V = 25 V
V = 5 V
IO = 15 mA to 700 mA

Figure 11

OUTPUT CURRENT† VS INPUT VOLTAGE

Tc = 0°C
Tc = 25°C
Tc = 125°C

† This is the minimum current required to maintain voltage regulation.

Figure 12
TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

LOAD TRANSIENT RESPONSE

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) generates 1.25 V nominal \( (V_{\text{ref}}) \) between OUT and ADJ. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

\[
V_O = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right) + I_{(ADJ)} (R_2)
\]

or

\[
V_O \approx V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right)
\]

The TL783 was designed to minimize the input current at ADJ and maintain consistency over line and load variations, thereby minimizing the associated \( (R_2) \) error term.

To maintain \( I_{(ADJ)} \) at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 \( \Omega \) provides a minimum load current of 15 mA. Larger values can be used when the input-to-output differential voltage is less than 125 V (see the output-current curve in Figure 14) or when the load sinks some portion of the minimum current.
DESIGN CONSIDERATIONS

bypass capacitors

The TL783 regulator is stable without bypass capacitors; however, any regulator becomes unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-μF tantalum or aluminum electrolytic capacitor usually is sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783 because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection presently is achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large load transient conditions. The addition of an output bypass capacitor greatly enhances load transient response and prevents dropout. For most applications, it is recommended that an output bypass capacitor be used, with a minimum value of:

\[ C_o \ (\mu F) = 15/V_o \]

Larger values provide proportionally better transient-response characteristics.

protection circuitry

The TL783 regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783 protect the device up to maximum-rated \( V_I \) as long as certain precautions are taken. If \( V_I \) is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, when rise times in excess of 10 V/ns are applied to the input, a parasitic npn transistor in parallel with the DMOS output can be turned on, causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as tantalum or aluminum electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater usually provides adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, when an instantaneous short circuit is applied to the output, both ringing and excessive fall times can result. A tantalum or aluminum electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of \( V_I \). A protective diode (see Figure 17) is required only for capacitance values greater than:

\[ C_o \ (\mu F) = 3 \times 10^4/(V_o)^2 \]

Care always should be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.
load regulation

The current-set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified, through the action of R1 and R2, to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.
APPLICATION INFORMATION

Figure 17. 1.25-V to 115-V Adjustable Regulator

Figure 18. 125-V Short-Circuit-Protected Off-Line Regulator

Figure 19. 50-V Regulator With Current Boost

Figure 20. Adjustable Regulator With Current Boost and Current Limit

† Needed if device is more than 4 inches from filter capacitor
APPLICATION INFORMATION

Figure 21. Current-Sinking Regulator

\[ I = \frac{V_{\text{ref}}}{R} \]

Load

TL783

IN

OUT

ADJ

\[ 1 \mu F \]

\[ R \]

Figure 22. Current-Sourcing Regulator

\[ I = \frac{V_{\text{ref}}}{R} \]

TL783

IN

OUT

ADJ

\[ 1 \mu F \]

\[ R \]

Load

Figure 23. High-Voltage Unity-Gain Offset Amplifier

\[ V_{\text{OFFSET}} = V_{\text{ref}} \left( I + \frac{R_2}{82} \right) \]

\[ V_{\text{CC}} \]

1 \mu F

TL783

IN

OUT

ADJ

\[ R \]

\[ 82 \Omega \]

TL081

\[ V+ \]

\[ V- \]

\[ \sim \]

\[ \sim \]

INPUT

OUTPUT

Figure 24. 48-V, 200-mA Float Charger

\[ V_I = 90 \text{ V} \]

\[ 82 \Omega \]

\[ 6.25 \Omega \]

\[ 3.9 \text{ k}\Omega \]

\[ 48 \text{ V} \]

TL783

IN

OUT

ADJ

TL783

IN

OUT

ADJ
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