General Description
Maxim's redesigned DG417/DG418/DG419 precision, CMOS, monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and guaranteed on-resistance flatness over the signal range (4Ω max). These switches conduct equally well in either direction and guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers low off-leakage current over temperature (less than 5nA at +85°C).

The DG417/DG418 are single-pole/single-throw (SPST) switches. The DG417 is normally closed, and the DG418 is normally open. The DG419 is single-pole/double-throw (SPDT) with one normally closed switch and one normally open switch. Switching times are less than 175ns max for tON and less than 145ns max for tOFF. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. The improved DG417/DG418/DG419 are fabricated with a 44V silicon-gate process.

New Features
- Plug-In Upgrades for Industry-Standard DG417/DG418/DG419
- Improved RDS(ON) Match Between Channels (3Ω max, DG419 only)
- Guaranteed RFLAT(ON) Over Signal Range (4Ω max)
- Improved Charge Injection (10pC max)
- Improved Off-Leakage Current Over Temperature (<5nA at +85°C)
- Withstand Electrostatic Discharge (2000V min) per Method 3015.7

Existing Features
- Low RDS(ON) (35Ω max)
- Single-Supply Operation +10V to +30V
- Bipolar-Supply Operation ±4.5V to ±20V
- Low Power Consumption (35µW max)
- Rail-to-Rail Signal Handling
- TTL/CMOS-Logic Compatible

Applications
Sample-and-Hold Circuits
Communications Systems
Test Equipment
Battery-Operated Systems
Modems
Fax Machines
Guidance and Control Systems
PBX, PABX
Audio Signal Routing
Military Radios

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DG417C</td>
<td>0°C to +70°C</td>
<td>8 Plastic DIP</td>
</tr>
<tr>
<td>DG417CY</td>
<td>0°C to +70°C</td>
<td>8 SO</td>
</tr>
<tr>
<td>DG417C/D</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
</tr>
<tr>
<td>DG417DJ</td>
<td>-40°C to +85°C</td>
<td>8 Plastic DIP</td>
</tr>
<tr>
<td>DG417DY</td>
<td>-40°C to +85°C</td>
<td>8 SO</td>
</tr>
</tbody>
</table>

Ordering Information continued at end of data sheet.
* Contact factory for dice specifications.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
Improved, SPST/SPDT Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
- \( V^+ \) ................................................................. 44V
- GND ................................. \((GND - 0.3V) \) to \((V^+ + 0.3V)\)
- VL .................................................. \((GND - 0.3V) \) to \((V^+ + 0.3V)\)
Digital Inputs \( V_S, V_D \) (Note 1) ...... \((V^- - 2V) \) to \((V^+ + 2V) \) or 30mA
- Continuous Current (any terminal) (Note 1) ........................................... 30mA
- Peak Current, S or D (pulsed at 1ms, 10% duty cycle max).................. 100mA
- Continuous Power Dissipation (\( T_A = +70^\circ C \))
- Plastic Dip (derate 9.09mW/°C above +70°C) .............................. 727mW
- SO (derate 5.88mW/°C above +70°C) ............................................. 471mW
- CERDIP (derate 8.00mW/°C above +70°C) ................................. 640mW
- Operating Temperature Ranges
  - DG41_C_ ............................................................. 0°C to +70°C
  - DG41_D_ .......................................................... -40°C to +85°C
  - DG41_AK........................................................ -55°C to +125°C
- Storage Temperature Range ............................................................ -65°C to +150°C
- Lead Temperature (soldering, 10sec) .............................................. +300°C

Note 1: Signals on S, D, or IN exceeding \( V^+ \) or \( V^- \) are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

\((V^+ = +15V, V^- = -15V, VL = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} \) to \( T_{MAX} \), unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Signal Range</td>
<td>( V_S, V_D )</td>
<td>(Note 3)</td>
<td>( TA = +25^\circ C )</td>
<td>( C, D )</td>
<td>20</td>
</tr>
<tr>
<td>Drain-Source On-Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>( V^+ = 13.5V, V^- = -13.5V, V_D = \pm 10V, I_S = -10mA )</td>
<td>( TA = T_{MIN} ) to ( T_{MAX} )</td>
<td></td>
<td>45</td>
</tr>
<tr>
<td>On-Resistance Match Between Channels (Note 4)</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>( V^+ = 15V, V^- = -15V, V_D = \pm 10V, I_S = -10mA )</td>
<td>( TA = +25^\circ C )</td>
<td></td>
<td>3</td>
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<tr>
<td>On-Resistance Flatness (Note 4)</td>
<td>( R_{FLAT(ON)} )</td>
<td>( V^+ = 15V, V^- = -15V, V_D = \pm 5V, I_S = -10mA )</td>
<td>( TA = +25^\circ C )</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>Source-Off Leakage Current (Note 5)</td>
<td>( I_{S(OFF)} )</td>
<td>( V^+ = 16.5V, V^- = -16.5V, V_D = \pm 15.5V, V_S = \mp 15.5V )</td>
<td>( TA = +25^\circ C )</td>
<td>( C, D )</td>
<td>-0.25</td>
</tr>
<tr>
<td>Drain-Off Leakage Current (Note 5)</td>
<td>( I_{D(OFF)} )</td>
<td>( V^+ = 16.5V, V^- = -16.5V, V_D = \pm 15.5V, V_S = \mp 15.5V )</td>
<td>( TA = +25^\circ C )</td>
<td>( C, D )</td>
<td>-0.4</td>
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<tr>
<td>Drain-On Leakage Current (Note 5)</td>
<td>( I_{D(ON)} )</td>
<td>( V^+ = 16.5V, V^- = -16.5V, V_D = \pm 15.5V, V_S = \mp 15.5V )</td>
<td>( TA = +25^\circ C )</td>
<td>( C, D )</td>
<td>-0.75</td>
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### ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, VINL = 0.8V, VINH = 2.4V, TA = TMIN to TMAX, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP (Note 2)</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td><strong>LOGIC INPUT</strong></td>
<td></td>
<td></td>
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<tr>
<td>Logic Input Current with Input Voltage High</td>
<td>INH</td>
<td>VIN = 2.4V</td>
<td>-0.5</td>
<td>0.005</td>
<td>0.5</td>
<td>µA</td>
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<tr>
<td>Logic Input Current with Input Voltage Low</td>
<td>INL</td>
<td>VIN = 0.8V</td>
<td>-0.5</td>
<td>0.005</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td><strong>DYNAMIC</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>tON</td>
<td>DG417/DG418, VD = ±10V, Figure 2</td>
<td>TA = +25°C</td>
<td>100</td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-Off Time</td>
<td>tOFF</td>
<td>DG417/DG418, VD = ±10V, Figure 2</td>
<td>TA = +25°C</td>
<td>60</td>
<td>145</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>210</td>
<td></td>
<td></td>
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<tr>
<td>Transition Time</td>
<td>tTRANS</td>
<td>DG419, VS = ±10V, Figure 3</td>
<td>TA = +25°C</td>
<td>175</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Break-Before-Make Interval</td>
<td>tD</td>
<td>DG419, VS1 = VS2 = ±10V, Figure 4, TA = +25°C</td>
<td></td>
<td>5</td>
<td>13</td>
<td>ns</td>
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<tr>
<td>Charge Injection (Note 3)</td>
<td>Q</td>
<td>VGEN = 0V, Figure 5, TA = +25°C</td>
<td></td>
<td>3</td>
<td>10</td>
<td>pC</td>
</tr>
<tr>
<td>Off-Isolation Rejection Ratio (Note 6)</td>
<td>OIRR</td>
<td>RL = 500Ω, CL = 5pF, f = 1MHz, Figure 6, TA = +25°C</td>
<td></td>
<td>68</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Crosstalk (Note 7)</td>
<td></td>
<td>DG419, RL = 500Ω, CL = 5pF, f = 1MHz, Figure 7, TA = +25°C</td>
<td></td>
<td>85</td>
<td></td>
<td>dB</td>
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<tr>
<td>Drain Off-Capacitance</td>
<td>CD (OFF)</td>
<td>VD = 0V, f = 1MHz, Figure 8, TA = +25°C</td>
<td></td>
<td>8</td>
<td></td>
<td>pF</td>
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<tr>
<td>Source Off-Capacitance</td>
<td>CS (OFF)</td>
<td>VD = 0V, f = 1MHz, Figure 8, TA = +25°C</td>
<td></td>
<td>8</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Drain-Source On-Capacitance</td>
<td>CD (ON) or CS (ON)</td>
<td>VS = 0V, f = 1MHz, Figure 9, TA = +25°C</td>
<td>DG417/DG418</td>
<td>30</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DG419</td>
<td>35</td>
<td></td>
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<td><strong>SUPPLY</strong></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Positive Supply Current</td>
<td>I+</td>
<td>V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V</td>
<td>TA = +25°C</td>
<td>-1</td>
<td>-0.0001</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Negative Supply Current</td>
<td>I-</td>
<td>V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V</td>
<td>TA = +25°C</td>
<td>-1</td>
<td>-0.0001</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Logic Supply Current</td>
<td>IL</td>
<td>V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V</td>
<td>TA = +25°C</td>
<td>-1</td>
<td>-0.0001</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Ground Current</td>
<td>IGROUND</td>
<td>V+ = 16.5V, V- = -16.5V, VIN = 0V or 5V</td>
<td>TA = +25°C</td>
<td>-1</td>
<td>-0.0001</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TA = TMIN to TMAX</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>
# Improved, SPST/SPDT Analog Switches

## ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, VL = 5V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = +25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP (Note 2)</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>SWITCH</td>
<td>VANALOG</td>
<td>(Note 3)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Drain-Source On-Resistance</td>
<td>RDS(ON)</td>
<td>IS = -10mA, VD = 3.8V, V+ = 10.8V</td>
<td>0</td>
<td>12</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Dynamic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>tON</td>
<td>DG417/DG418, VD = 8V, Figure 2</td>
<td>110</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Time</td>
<td>tOFF</td>
<td>DG417/DG418, VD = 8V, Figure 2</td>
<td></td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Break-Before-Make Interval</td>
<td>td</td>
<td>DG419, RL = 1000Ω, CL = 35pF, Figure 4</td>
<td></td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Charge Injection (Note 3)</td>
<td>Q</td>
<td>CL = 10nF, VGEN = 0V, RGEN = 0V, Figure 5</td>
<td></td>
<td>2</td>
<td>10</td>
<td>pC</td>
</tr>
<tr>
<td>Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Supply Current</td>
<td>I+</td>
<td>All channels on or off, V+ = 13.2V, VL = 5.25V, VIN = 0V or 5V</td>
<td>-0.0001</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Negative Supply Current</td>
<td>I-</td>
<td>All channels on or off, V+ = 13.2V, VL = 5.25V, VIN = 0V or 5V</td>
<td>-0.0001</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Logic Supply Current</td>
<td>IL</td>
<td>All channels on or off, VL = 5.25V, VIN = 0V or 5V</td>
<td>-0.0001</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Ground Current</td>
<td>IGND</td>
<td>All channels on or off, VL = 5.25V, VIN = 0V or 5V</td>
<td>-0.0001</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

**Note 2:** Typical values are for design aid only, are not guaranteed, and are not subject to production testing. The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:** On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

**Note 5:** Leakage parameters IS(OFF), ID(OFF), and ID(ON) are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

**Note 6:** Off-Isolation Rejection Ratio = 20log (VD/Vs), VD = output, Vs = input to off switch.

**Note 7:** Between any two switches.
Improved, SPST/SPDT Analog Switches

Typical Operating Characteristics

(TA = +25°C, unless otherwise noted.)

- **ON-RESISTANCE vs. VD AND POWER-SUPPLY VOLTAGE**
  - A: V+ = 5V, V- = -5V
  - B: V+ = 10V, V- = -10V
  - C: V+ = 15V, V- = -15V
  - D: V+ = 20V, V- = -20V

- **ON-RESISTANCE vs. VD AND TEMPERATURE**
  - V+ = 15V
  - V- = -15V
  - TA = +125°C
  - TA = +85°C
  - TA = +25°C
  - TA = -55°C

- **OFF-LEAKAGE CURRENT vs. TEMPERATURE**
  - V+ = 15V
  - V- = -15V
  - VD = ±15V
  - VS = ±15V

- **ON-LEAKAGE CURRENT vs. TEMPERATURE**
  - V+ = 16.5V
  - V- = -16.5V
  - VD = ±15V
  - VS = ±15V

- **SUPPLY CURRENT vs. TEMPERATURE**
  - A: I+ at V+ = 16.5V
  - B: I- at V- = -16.5V
  - C: IL at VS = 5V

- **CHARGE INJECTION vs. ANALOG VOLTAGE**
  - V+ = 15V
  - V- = -15V
Improved, SPST/SPDT Analog Switches

Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
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<tr>
<td>1</td>
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</tr>
<tr>
<td>—</td>
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<td>S</td>
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<td>—</td>
<td>—</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>N.C.</td>
</tr>
<tr>
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<td>—</td>
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</table>

**Applications Information**

**Operation with Supply Voltages Other than ±15V**

Using supply voltages other than ±15V reduces the analog signal range. The DG417/DG418/DG419 switches operate with ±4.5V to ±20V bipolar supplies or with ±10V to ±30V single supply: connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies, such as +24V and -5V. V+ must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The Typical Operating Characteristics graphs show typical on-resistance with ±20V, ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

**Overvoltage Protection**

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to 1V below V+ and 1V above V- without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.
Improved, SPST/SPDT Analog Switches

Test Circuits/Timing Diagrams

Figure 2. DG417/DG418 Switching Time

Figure 3. DG419 Transition Time
Improved, SPST/SPDT Analog Switches

Test Circuits/Timing Diagrams (continued)

Figure 4. DG419 Break-Before-Make Interval

Figure 5. Charge Injection
Improved, SPST/SPDT Analog Switches

Figure 6. Off-Isolation Rejection Ratio

Figure 7. DG419 Crosstalk

Figure 8. Drain-Source Off-Capacitance

Figure 9. Drain-Source On-Capacitance
Improved, SPST/SPDT Analog Switches

*Ordering Information (continued)*

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DG417DK</td>
<td>-40°C to +85°C</td>
<td>8 CERDIP</td>
</tr>
<tr>
<td>DG417AK</td>
<td>-55°C to +125°C</td>
<td>8 CERDIP**</td>
</tr>
<tr>
<td>DG418CJ</td>
<td>0°C to +70°C</td>
<td>8 Plastic DIP</td>
</tr>
<tr>
<td>DG418CY</td>
<td>0°C to +70°C</td>
<td>8 SO</td>
</tr>
<tr>
<td>DG418C/D</td>
<td>0°C to +70°C</td>
<td>Dice*</td>
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* Contact factory for dice specifications.
** Contact factory for availability and processing to MIL-STD-883B.

Chip Topography

TRANISTOR COUNT: 32
SUBSTRATE CONNECTED TO V+

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Improved, SPST/SPDT Analog Switches

Package Information
Improved, SPST/SPDT Analog Switches

Package Information (continued)

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